\chapter{Design of Ring Oscillator

}

\label{ch:chap1}

\section{Objective}

The objective of this assignment is to gain a comprehensive understanding of the design principles associated with ring oscillators using CMOS technology. The primary focus is on utilizing LT Spice XVII, an open-source simulation tool, to design a ring oscillator circuit based on NOT gates.

\section{Procedure}

\section\*{STEP-1}

\begin{enumerate}

\item Launch LT-Spice simulator.

\item Design a CMOS inverter circuit using \texttt{pmos4} and \texttt{nmos4} transistors. Set the supply voltage to be 5V and apply 0-5V 100MHz pulses at the input of the inverter.\\

Some transistors may have many parameters in common. Instead of defining transistor parameters for every instance, transistors are grouped by model name and have parameters in common. The transistors of the same model can have different sizes, and the electrical behavior is scaled to the size of the instance.\\

\\

Syntax: \texttt{.model <modname> <type>[(<parameter list>)]}\\

You may set the transistor parameters by selecting: \texttt{EDIT -> SPICE DIRECTIVES}\\

\textbf{NMOS Transistor:}

\begin{verbatim}

.MODEL CMOSN NMOS KP=96u VTO=0.786 LAMBDA=0.01 TOX=21n GAMMA=0.586

\end{verbatim}

\textbf{PMOS Transistor:}

\begin{verbatim}

.MODEL CMOSP PMOS KP=96u VTO=-0.906 LAMBDA=0.01 TOX=21n GAMMA=0.486

\end{verbatim}

\textbf{Please note the minus sign and units carefully. \texttt{CMOSN} and \texttt{CMOSP} are the model names for the Transistors, and do not use \texttt{NMOS} or \texttt{PMOS} as model names.}\\

\texttt{KP – Transconductance Parameter (A/V\textsuperscript{2})}\\

\texttt{VTO – Zero-bias threshold voltage (V)}\\

\texttt{LAMBDA – Channel-length modulation (1/V)}\\

\texttt{TOX – Oxide Thickness (m)}\\

\texttt{GAMMA – Bulk threshold parameter (V\textsuperscript{1/2})}

\item Measure the gate delay of the NOT gate.\\

\[

\text{Rise/fall time} = 0.1 \, \text{ns}

\]

\[

t\_{pLH} = 280 \, \text{ps}

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\[

t\_{pHL} = 430 \, \text{ps}

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\[

\text{Gate delay} = \frac{t\_{pLH} + t\_{pHL}}{2} = 355 \, \text{ps}

\]

\begin{figure}[h]

\centering

\includegraphics[width=1\textwidth]{results\_Page\_1\_Image\_0001.png}

\caption{}

\label{fig: }

\end{figure}

\item How do you justify your reading?

\item Why is the PMOS transistor width selected almost twice that of NMOS transistor?

\item Observe the effect by setting the same width (100u) for both PMOS and NMOS transistors.

\end{enumerate}

\begin{figure}[h]

\centering

\includegraphics[width=1\textwidth]{results\_Page\_1\_Image\_0002.png}

\caption{The effect by setting the same width (100u) for both PMOS and NMOS transistors}

\label{fig: }

\end{figure}

\[

t\_{pLH} = 337 \, \text{ps}

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\[

t\_{pHL} = 315 \, \text{ps}

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\section\*{STEP-2}

\begin{enumerate}

\item Add the parasitic capacitances for PMOS and NMOS transistors. You may add these values in your model directives.

\textbf{NMOS Transistor:}

\begin{verbatim}

CGDO=402p CGSO=402p CGBO=362p

\end{verbatim}

\textbf{PMOS Transistor:}

\begin{verbatim}

CGDO=54p CGSO=54p CGBO=336p

\end{verbatim}

CGDO – Gate-drain overlap capacitance per meter channel width (F/m) \\

CGSO – Gate-source overlap capacitance per meter channel width (F/m) \\

CGBO – Gate-bulk overlap capacitance per meter channel width (F/m)

\begin{figure}[h]

\centering

\includegraphics[width=1\textwidth]{inverter.png}

\caption{NOT gate}

\label{fig: }

\end{figure}

\item Measure the gate delay.\\

\[

t\_{pLH} = 287 \, \text{ps}

\]

\[

t\_{pHL} = 444 \, \text{ps}

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\[

\text{Gate delay} = 365.5 \, \text{ps}

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\begin{figure}[h]

\centering

\includegraphics[width=1\textwidth]{results\_Page\_2\_Image\_0001.png}

\caption{}

\label{fig: }

\end{figure}

\item Justify your reading with engineering background.

\item Observe the effect on frequency, rise time, and fall time of the designed NOT gate by changing L and W parameters of the PMOS and NMOS transistors.

\begin{table}[h]

\centering

\begin{tabular}{|c|c|c|c|c|c|c|}

\hline

NMOS & PMOS & $t\_{pLH}$ & $t\_{pHL}$ & Delay & Rise time & Fall time \\

\hline

10, 100 & 10, 200 & & & 365.5 & 747 ps & 750 ps \\

\hline

10, 100 & 10, 100 & 356.4 & 356.4 & 356.4 & 766 ps & 700 ps \\

\hline

10, 50 & 10, 100 & 294 & 454 & 762 & 762 & \\

\hline

15, 100 & 15, 200 & 560 & 945 & 1676 & 1645 & \\

\hline

5, 100 & 5, 200 & 111 & 156 & 210 & 217 & \\

\hline

10, 150 & 10, 300 & 263 & 441 & 767 & 777 & \\

\hline

\end{tabular}

\end{table}

\end{enumerate}

\section\*{STEP-3}

\begin{enumerate}

\item Choose one odd number between 3 and 11. Say your choice is \(N\) \{3, 5, 7, 9, or 11\}.

\item Copy the NOT gate designed in STEP-2 and place \(N\) times one after another in a row. Connect the inputs and outputs of the NOT gates to form a Ring Oscillator. Connect the \(V\_{DD}\) and \(GND\) as well.

\begin{figure}[h]

\centering

\includegraphics[width=1\textwidth]{ringoscilator.png}

\caption{Ring Oscillator}

\label{fig: }

\end{figure}

\item Observe the waveform. Adjust the transistor parameters to get a reasonably good waveform with reasonably good clock properties such as rise time, fall time, and duty cycle.

\begin{figure}[h]

\centering

\includegraphics[width=1\textwidth]{results\_Page\_2\_Image\_0002.png}

\caption{Ring Oscillator}

\label{fig: }

\end{figure}

\item Add an additional inverter at the output of the Ring Oscillator to smooth the output waveform.

\begin{figure}[h]

\centering

\includegraphics[width=1\textwidth]{ringoscillatorfull.png}

\caption{Add an additional inverter at the output of the Ring Oscillator}

\label{fig: }

\end{figure}

\begin{figure}[h]

\centering

\includegraphics[width=1\textwidth]{results\_Page\_2\_Image\_0003.png}

\caption{Add an additional inverter at the output of the Ring Oscillator}

\label{fig: }

\end{figure}

\end{enumerate}

\[

\text{Fall time} = 1.52 \, \text{ns}

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\[

\text{Rise time} = 2.27 \, \text{ns}

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\endinput